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Date: 2/15/2011

Message: RE: In-Person Interview on Friday, 2/18, re US App. No. 10/550,323 (Attorney Docket 53047-57370)

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Total Number of Pages, including this page: 3

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DRAFT – FOR DISCUSSION PURPOSES ONLY

To: Examiner Jean Fleurantin
From: Ben Volk
Re: In-Person Interview on Friday (2/18) at 1 PM re US Pat. App. Ser. No. 10/550,323
(Attorney Docket 53047-57370)

INTERVIEW AGENDA FOR 10/550,323

1. Explain background and nature of the invention.

2. Discuss the shortcomings of the cited references.
   - Relative to independent claims 40, 54, 100, and 102, the Dixon and Villasenor references fail to disclose, teach or suggest a multi-functional pipeline deployed on a reconfigurable logic device formed by a plurality of pipelined data processing engines, whereby a control processor activates/deactivates the data processing engines as desired to achieve an overall pipeline function. The Office Action cites Villasenor for alleged teachings relating to the feature whereby the pipelined data processing engines are activated/deactivated as desired to achieve an overall pipeline function. However, a close inspection of Villasenor reveals that Villasenor does not teach the use of activation/deactivation control signals to define the function of a reconfigurable logic device. Instead, Villasenor changes the function of the reconfigurable logic device by reconfiguring the FPGA. This means that Villasenor does not turn data processing engines on or off using a control signal. Instead, Villasenor writes a new hardware template to the FPGA to completely remove data processing operations that are not needed for a particular operation and add data processing operations that are needed. By contrast, the claimed invention avoids the time-consuming act of FPGA reconfiguration by more simply using a control processor to activate/deactivate the pipelined data processing engines, thereby reducing the amount of time needed to change the overall function for the subject pipeline. With the claimed invention, if a data processing engine is deactivated, its logic is still present on the reconfigurable logic device (unlike Villasenor).

   - Relative to dependent claims 49, 105, 142, and 166, Applicant notes that the cited references fail to disclose, teach or suggest the subject multi-functional pipeline where one of the data processing engines is a data reduction engine. In particular, the cited references fail to disclose, teach or suggest a data reduction engine within a multi-functional pipeline wherein the data reduction engine is configured to operate on streaming financial information. The Office Action's citation to the background section of the patent application fails to render these claims obvious in combination with the other cited references. While the background section describes the indexing of financial information, it does not hint at the use of a data reduction engine implemented as part of a multi-functional pipeline on a reconfigurable logic device that can be activated/deactivated by a control processor to define an overall function for the pipeline.

   - Relative to dependent claims 137 and 161, Applicant notes that the Dixon/Villasensor combination fail to render obvious the concept of activating and deactivating the

pipelined data processing engines differently to change the pipeline function based on a direction of data flow through the pipeline (e.g., , to or from storage)). That is, for data flowing in one direction through the pipeline, a different set of data processing engines will be activated/deactivated than they would for data flowing in the other direction through the pipeline.

- Relative to dependent claims 41 and 55, the Dixon/Villasenor/Wong combination fails to render obvious the concept of activating a decryption engine and a downstream search engine the multi-functional pipeline to enable crypto-searching. The shortcomings of Dixon and Villasenor are already as noted above. Applicant further notes that the addition of Wong to the citation does not bridge the gaps left by Dixon and Villasenor. Wong merely teaches that the bitfile used to configured an FPGA can be encrypted during transmission to the FPGA and decrypted prior to the bitfile being used to reconfigure the FPGA. Wong, in isolation or in combination with the other cited references, does not contemplate pipelining a decryption operation with a downstream search operation to enable searches within the decrypted data.